REMARKS

The Office Action dated September 21, 2009, indicated that claims 1-7, 9-17, 32-36, 39 and 43 stand rejected under 35 U.S.C. § 102(b) over Akimoto *et al.* (U.S. Pub. 2002/0117689); claims 30-31 and 37 stand rejected under 35 U.S.C. § 102(b) over Akimoto; claim 38 stands rejected under 35 U.S.C. § 102(b) over Mizutani *et al.* (U.S. 5,616,944); claim 8 stands rejected under 35 U.S.C. § 103(a) over Akimoto as applied to claim 1, and further in view of Baba (US 5,589,696); and claims 21-29 stand rejected under 35 U.S.C. § 103(a) over Mizutani as applied to claim 1, and further in view of Baba.

Applicant respectfully traverses each of the rejections, and in the discussion set forth below, does not acquiesce to any rejection or averment in this Office Action or the Office Action(s) of record unless Applicant expressly indicates otherwise. Moreover, as the Office Action has not directly addressed various issues identified in Applicant's traversals, including those involving the teaching away/undermining of purpose as effected via the (unsupported) combination of references under § 103, and as the rejections continue to rely upon unsupported allegations of "inherent" functions (contrary to applicable case law and the M.P.E.P.), Applicant further incorporates its traversals of record herein.

Specifically regarding the '689 reference, the disclosed structures appear to be directed to overcome limitations of polysilicon when used in a conventional MOS device. However, the reference fails to contemplate the claimed invention and fails to mention aspects including reverse bias operation, avalanche breakdown, impact ionization and related embodiments as relative, for example, to turn on slopes well below 60 mV/decade. Accordingly, the '689 reference fails to correspond as asserted in the Office Action.

Notwithstanding the above, Applicant has amended certain claims in a manner that is believed to be consistent with the claims as previously presented and with the discussed aspects of the claimed invention. Applicant believes that the cited references are inapplicable to the claims as amended. Referring to claim 1 by way of example, limitations are directed to a control circuit that applies a control signal, to effect operation of the device as previously claimed. As consistent with the Examiner's earlier indications regarding this subject matter (and what the claimed gate is configured to do – see page 3 of the Office Action), Applicant believes that amended claim 1 is allowable over the cited references as the references (alone or in combination) fail to teach or suggest limitations directed to effecting a change in carriers of an

intrinsic region, relative to a first junction and offset from another junction. Moreover, the cited references fail to contemplate or recognize the applicability of such limitations in the context of devices such as those involved in logic or memory for rapid switching applications. Related amendments have been made to claims that depend from claim 1 for consistency. Support for these amendments may be found throughout the specification and figures, with exemplary embodiments shown in FIG. 11 (*see*, *e.g.*, items 1130 and 1140) and described in the corresponding discussion.

Similar amendments have been made to each of the independent claims, and related amendments have been made to the claims that depend therefrom, also for consistency. Accordingly, Applicant believes that the rejections are no longer applicable and that the claims are in condition for allowance.

In addition to the above, the following addresses errors in the proposed combination of references and in the alleged correspondence, and further summarizes traversals as previously presented in the record, as applicable to the lack of correspondence between the cited references and one or more claim limitations as presented herein.

Applicant maintains that the rejections over the '944 reference are improper because the '944 reference fails to disclose limitations directed to controlling an electric field distribution in an intermediate region of a semiconductor device for rapid switching. While the cited portions of the '944 reference discuss a diode structure having a gate-controlled electric field distribution, the gate is centered upon an intrinsic region, the operation of the gate evenly affects the potential of the impurity region 16 "as a whole" (rather than closer to one or another junction as claimed; *see* column 5:43-44), and implementation of the gate generally fails to comprehend or disclose various aspects of the claimed invention. Moreover, nothing in the '944 reference suggests the application of control signals (as claimed above). For example, the '944 reference (alone or in combination) fails to disclose limitations directed to structure and operation for rapid transitioning between ON and OFF states, including limitations directed to the use of a gate that is offset to affect the electric field at one of the junctions (*i.e.*, at one of the junctions in a P-I-N structure) as shown, for example, in FIG. 1A.

Related limitations may be found in a multitude of independent claims. For example, regarding claim 38 as rejected under § 102 over the '944 reference, the reference fails to disclose limitations directed to presenting "an electric field substantially at only one of the first and

second junctions." This is also consistent with the Examiner's previous indications that "Mizutani does not teach a gate offset to present an electric field substantially at only one of the two junctions." The '944 reference also does not disclose or even mention an avalanche breakdown (*e.g.*, as in claim 2), which is achievable using such an approach.

While further discussion of the § 103 rejections is believed unnecessary in view of the above, Applicant submits that the Office Action's stated rationale for adding the secondary '696 reference (to either the newly-cited '689 reference or the previously-cited '944 reference) to "have the gate located predominantly over the second region to be more highly integrated as taught by" is inapplicable because the '696 reference does not involve effecting an electric field distribution near a junction, and the rejections have not established that the proposed combination would (or could) operate in such a manner. Similarly, the rejections have not established that the proposed combination with the '696 reference would "create and offset current at only one of the two junctions in the reverse biased mode" as suggested at pages 16-17 of the instant Office Action. For example, cited Figure 2 discloses a tunnel transistor in which a gate is located over a heavily-doped degenerative region (N+ region 27), and not over any intrinsic region as claimed. Moreover, the gate 21 is not arranged to cause a field distribution as claimed, and if implemented with the '944 reference, does not appear to be capable of introducing a breakdown condition via channel length adjustment.

Applicant further submits that any modification of the '944 reference to include offset gate structures and/or functions relating to effecting a carrier concentration in an offset portion of an intrinsic region is unmotivated because the '944 reference teaches away from such a modification, and further because such modification would appear to render the '944 reference inoperable for its purpose. Consistent with the recent Supreme Court decision, M.P.E.P. § 2143.01 explains the long-standing principle that a § 103 rejection cannot be maintained when the asserted modification undermines either the operation or the purpose of the main (AAPA) reference - the rationale being that the prior art teaches away from such a modification. *See KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1742 (2007) ("[W]hen the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious."). *See also In re Gordon*, 733 F.2d 900 (Fed. Cir. 1984) (A §103 rejection cannot be maintained when the asserted modification undermines purpose of the main reference.). In this instance, modifying the gate structure and/or

its application of the '944 reference (see FIG. 5A) would undermine its purpose of affecting the potential of an impurity region "as a whole" per the above discussion. In accordance with the aforesaid purpose, the '944 reference thus teaches away from the claimed invention.

In view of the above, all of the §§ 102 and 103 rejections are believed to be improper, and Applicant requests that they be removed. Applicant therefore believes that each of the rejections is overcome, and that the application is in condition for allowance. A favorable response is requested. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is encouraged to contact the undersigned at (651) 686-6633.

Respectfully submitted,

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Dated: December 16, 2009

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